REMARKS/ARGUMENTS

This responds to the Office Action, dated August 7, 2006. Claims 1 - 67 are pending in this application.

Claim Rejections - 35 USC § 103

The Examiner rejected Claims 1-4, 14, 42-44, 46, 47, 49-52, 54, and 58-61 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,150,619 to Reynolds in view of U.S. Patent No. 6,301,649 to Takasugi, and further in view of U.S. Patent No. 6,496,192 to Shreesha, and in view of what the Examiner considers to be Applicant-admitted prior art. Applicants respectfully traverse these rejections.

Regarding claim 1, the Examiner cited Reynolds in view of Takasugi and Shreesha as grounds for his rejection. Claim 1 recites in part, for example, that at least two data elements that are consecutive in a first order be stored in parallel to at least two memory devices and at least two data elements that are consecutive in a second order be retrieved in parallel from the at least two memory devices. The Examiner has noted that Reynolds does not disclose the storage and retrieval of consecutive data units in parallel and instead relies on Takasugi. As to Takasugi, the Examiner stated that while Takasugi does not disclose the storage of data elements that are consecutive, it does disclose the storage and retrieval of data elements in parallel. In support of this, col. 9, lines 60-64 of Takasugi were cited and the Examiner described a certain circuitry arrangement shown therein.

However, this cited portion of Takasugi merely refers to FIG. 14 and discusses an I/O circuit having an I/O terminal that is electrically connected to the data bus pairs so as to perform a common input/output operation between two banks. There is no discussion or suggestion that this I/O terminal operates to store in parallel at least two data elements or the retrieval in parallel of two data elements as recited in claim 1. Moreover, the other cited portions of Takasugi only disclose a memory comprised of a plurality of banks that uses bank interleaving and specifically describes that data elements are not stored or retrieved in parallel but instead are stored or retrieved individually in serial. It describes an ability to obtain a high-speed serial access to continuous address bits on different rows to thereby

operate write addresses. As a result, the continuous high-speed serial access in the column direction can be performed by the memory.

Specifically, for example, the Takasugi reference states in describing the writing of data to a single memory having a memory array comprised of a plurality of banks, bank-0 and bank-1, that:

> D(0, 0) is first written into the leading bit in B(0, 0) of La(0). D(0, 1) is secondly written into the leading bit in B(1, 0) of La(1). Further, D(0, 2) is thirdly written into the leading bit in B(2, 0) of La(2). The same operation as described above is repeated and thereafter....
> (Takasugi, col. 5, lines 55-59, emphasis added).

The Takasugi patent makes it clear that the writing of bits is performed in alternative writes, and does not write two bits in parallel. Takasugi further states that "bank-0 and bank-1 are alternatively accessed even in the case of the serial access in the column direction" (Takasugi, col. 9, lines 32-33, emphasis added). This non-parallel, alternating pattern is described throughout the Takasugi patent (e.g., see column 8, lines 51-59 stating "D(0, 0) ... is first written into the leading bit in B(0, 0) of La(0) ... Secondly, D(0, 1) is written into the leading bit in B(1, 0) of La(1). Thirdly, D(0, 2) is written into the leading bit in B(2, 0) of La(2). Further, D(0, 3) is written into the leading bit in B(3, 0) of La(3) as the fourth...." (emphasis added), see also at least column 6, lines col. 6, and 57-61. Further, the Takasugi patent continues stating "[w]hile the write operation is being performed at the above bank-0, the bank-1 is ready for its writing. Getting ready for the writing includes precharging one of the bit lines of the bank-1" (Takasugi, col. 5, lines 64-67, emphasis added), making it clear that each bit is written separately in an alternating manner and does not teach or suggest writing in parallel.

Similarly, the Takasugi patent does not teach or suggest retrieving data in parallel but instead serially in an alternating order. Specifically, the Takasugi patent states that "[t]he read operation can be performed in exactly the same manner as the write operation..." (col. 7, lines 26-27, emphasis added). Further, at column 7, lines 53-67 the Takasugi patent describes that "[t]his D(0, q) will first be read as the leading bit. Similarly, the next read data D(1, q) is equivalent to data positioned next to D(0, q) in B(q, 0) of La(q) in the bank-1. This data is read as the second read data...." (emphasis added)

Therefore, it is clear that the Takasugi patent does not teach parallel storing or retrieving, and instead teaches away from parallel storing and retrieving in that the data is serially written or read.

Therefore, the cited portions of Takasugi disclose serial access to image data, but not the parallel storing and retrieving as described in claim 1. That is, these cited portions do not show two data elements that are consecutive in the first order stored in parallel to the memory devices, and two data elements that are consecutive in the second order retrieved in parallel from the memory devices.

Similarly, the cited portions of Shreesha do not disclose this parallel storing and retrieving requirement. In the cited portions of Shreesha, a memory system operates by storing several adjacent pixel elements along one dimension of the image into the memory in a single first memory write operation. While this first write operation is being performed to one bank of the memory device, the next subsequent pixel elements are being prepared to be written into the other bank of the memory device. Thus the parallel storing and retrieving requirement of claim 1 is not present in the cited portions of Shreesha.

Because the cited portions of neither Reynolds, Takasugi nor Shreesha disclose this parallel storing of data elements that are consecutive in the first order and parallel retrieving of data elements that are consecutive in the second order, this claim is not rendered obvious by their combination.

Further, one skilled in the art would not combine at least the Shreesha patent with at least the Takasugi patent. The office action relies on Takasugi as the basis for parallel storing and retrieve. As demonstrated above, the Takasugi patent does not teach parallel storing and retrieving, and instead is specifically designed to alternatively store bit information between two banks. It would defeat the intended purpose of the Takasugi patent in that it is the "object of the [Takasugi patent] to provide a memory device allowing only memories capable of providing quick serial access in a row direction to obtain quick serial access in a column direction" (col. 2, lines 19-22). To achieve this serial access, the Takasugi patent incorporates an elaborate data storage sequence such that consecutive bits are distributed between separate portions (La and Lb) of memory array comprised of a plurality of banks, bank-0 and bank-1. For example, at least FIGS. 4-6 and the description of FIGS. 4-6 clearly demonstrate that consecutive data bits are purposely distributed over the

two memory banks to achieve the desired access. The Shreesha patent alternatively describes sequentially accessing an entire memory row of adjacent pixel elements. Specifically, the Shreesha patent states "when any memory cell in a memory bank is accessed, the entire memory row in the bank which includes that cell is transferred to the cache memory" (Shreesha, col. 4, lines 27-30, emphasis added). Therefore, to require the Takasugi patent to transfer the entire memory row in the bank would defeat the intended purpose of Takasugi as such operation would destroy the ability to achieve the series assess as described.

Moreover, Applicant respectfully contends that it was not proper to combine Takasugi with Reynolds, nor was it proper to combine Shreesha with Reynolds and Takasugi. In order to combine references, the Examiner is required to show that there was a teaching, suggestion, or motivation to combine them. The reason given by the Examiner for combining Reynolds with Takasugi is because Takasugi provides for "quick access in row or column directions thus reducing data transfer latency." (Office Action, pages 2, 4) The reason given for combining Shreesha with the combination of Reynolds and Takasugi is that Shreesha "allows blocks of image data to be fetched without latency." Additionally the Examiner stated that Shreesha "provides for improving memory operations." (Office Action, pages 2, 5)

However, Applicants respectfully submit that this is not the sort of valid teaching, suggestion, or motivation required by controlling Federal Circuit law. The reasons given in the Office Action merely state what the Examiner considers each of the references to disclose. There is no showing why one skilled in the art would be motivated to combine them, or where there is a valid teaching or suggestion to do so. Accordingly the reasons listed in the Office Action are conclusory. As stated by the Federal Circuit Court of Appeals in Cardiac Pacemakers, Inc., v. St. Jude Medical, Inc., 381 F.3d 1371 (Fed. Cir. 2004):

> "Recognition of a need does not render obvious the achievement that meets that need. There is an important distinction between the general motivation to cure an uncured disease (for example, the disease of multiple forms of heart irregularity), and the motivation to create a particular cure."

In our case, the cited portions of Takasugi generally deal with an ability to obtain a high-speed serial access to continuous address bits on different rows to thereby operate write addresses, so that high-speed serial access in the column direction can be performed by the

memory. The cited portions of Shreesha generally deal with the filtering or re-sizing of images and acknowledge a need to filter the image data faster. However, the mere recognition of these needs by Takasugi or Shreesha does not render obvious Applicant's particular invention in claim 1 for achieving greater speed, *i.e.,* including the storing and retrieving of consecutive data elements in parallel in two different orders. Therefore, there was no basis to combine Reynolds with Takasugi, and there was no basis to combine Shreesha with Reynolds and Takasugi. Thus for this additional reason, claim 1 is not obvious under Reynolds in view of Takasugi and Shreesha. Withdrawal of the rejection to claim 1 is requested.

Claims 2 - 46 depend directly or indirectly from claim 1, and include all limitations of claim 1. Having established that claim 1 was not rendered obvious in view of the cited references, dependent claims 2 - 46 similarly are not obvious. Withdrawal of the rejections to claims 2 - 46 also is requested.

Regarding independent claim 47, the Examiner cited Reynolds in view of Takasugi and Shreesha as grounds for his rejection, incorporating the same arguments as those used in rejecting claim 1. Claim 47 provides in part, for example, that at least two pixels that are horizontally adjacent are stored in parallel, and that at least two pixels that are vertically adjacent are retrieved in parallel. Because the cited portions of neither Reynolds, Takasugi nor Shreesha disclose this parallel storing of horizontally adjacent pixel data and parallel retrieving of vertically adjacent pixel data, (as discussed more fully above in connection with claim 1) claim 47 is not rendered obvious by their combination. Additionally, for the reasons discussed above, it was not proper to combine Takasugi with Reynolds, nor was it proper to combine Shreesha with Reynolds and Takasugi, because there was no adequate showing of a teaching, suggestion, or motivation to combine them. Withdrawal of the rejection to claim 47 is requested.

Claims 48 - 50 depend directly or indirectly from claim 47, and include all limitations of claim 47. Having established that claim 47 was not rendered obvious in view of the cited references, dependent claims 48 - 50 similarly are not obvious. Withdrawal of the rejections to claims 48 - 50 also is requested.

Regarding independent claim 51, the Examiner cited Reynolds in view of Takasugi and Shreesha as grounds for his rejection, incorporating the same arguments as those used in

rejecting claim 1. Claim 51 provides, at least in part, that a buffer stores multiple data elements in parallel to respective memory pages according to the first order and retrieves multiple data elements in parallel from respective memory pages according to the second order. Because the cited portions of neither Reynolds, Takasugi nor Shreesha disclose parallel storing by a buffer according to the first order and parallel retrieving by the buffer according to the second order, this claim is not rendered obvious by their combination. Additionally, for the reasons discussed above in connection with claim 1, it was not proper to combine Takasugi with Reynolds, nor was it proper to combine Shreesha with Reynolds and Takasugi, because there was no adequate showing of a teaching, suggestion, or motivation to combine them. Withdrawal of the rejection to claim 51 is requested.

Claims 52 - 58 depend directly or indirectly from claim 51, and include all limitations of claim 51. Having established that claim 51 was not rendered obvious in view of the cited references, dependent claims 52 - 58 similarly are not obvious. Withdrawal of the rejections to claims 52 - 58 also is requested.

Regarding independent claim 59, the Examiner cited Reynolds in view of Takasugi and Shreesha as grounds for his rejection, incorporating the same arguments as those used in rejecting claim 1. Claim 59 provides, for example, that a memory controller stores pixel data for multiple pixels in parallel to respective memory pages according to pixel pages and retrieves pixel data for multiple pixels in parallel from respective memory pages according to pixel pages. Because the cited portions of neither Reynolds, Takasugi nor Shreesha disclose this parallel storing and retrieving requirement of claim 59, this claim is not rendered obvious by their combination. Additionally, for the reasons discussed above in connection with claim 1, it was not proper to combine Takasugi with Reynolds, nor was it proper to combine Shreesha with Reynolds and Takasugi, because there was no adequate showing of a teaching, suggestion, or motivation to combine them. Withdrawal of the rejection to claim 59 is requested.

Regarding independent claim 60, the Examiner cited Reynolds in view of Takasugi and Shreesha as grounds for his rejection, incorporating the same arguments as those used in rejecting claim 1. Claim 60, however, provides at least in part for storing a first pixel and a second pixel in parallel in a first memory and a second memory, respectively, and storing a third pixel and a fourth pixel in parallel in the second memory and the first memory,

respectively. The first pixel is the leftmost pixel in the first horizontal row of pixels and the second pixel is horizontally adjacent to the first pixel. The third pixel is the leftmost pixel in the second horizontal row of pixels and is vertically adjacent to the first pixel. The fourth pixel is horizontally adjacent to the third pixel. The first and fourth pixels are stored in the same memory page in the first memory, whereas the second and third pixels are stored in the same memory page in the second memory.

The cited portions of neither Reynolds, Takasugi nor Shreesha disclose this parallel storing of claim 60 in the recited fashion, and therefore this claim is not rendered obvious by their combination. Additionally, for the reasons discussed above in connection with claim 1, it was not proper to combine Takasugi with Reynolds, nor was it proper to combine Shreesha with Reynolds and Takasugi, because there was no adequate showing of a teaching, suggestion, or motivation to combine them. Withdrawal of the rejection to claim 60 is requested.

Claim 61 depends directly from claim 60, and includes all limitations of claim 60. Having established that claim 60 was not rendered obvious in view of the cited references, dependent claim 61 similarly is not obvious. Withdrawal of the rejection to claim 61 also is requested.

The Examiner rejected independent claims 62 and 64-67 under 35 U.S.C. §103(a) as being unpatentable over Reynolds in view of Takasugi, and further in view of Shreesha, and further in view of what the Examiner considers Applicant-admitted prior art as applied to claim 1 above and further in view of U.S. Patent No. 6,018,354 to Jones and further in view of U.S. Patent No. 6,724,396 to Emmot. Certain other claims, which are dependent claims, were also rejected in view of these references. However those other claims have already been addressed above.

As a preliminary note, no less than five (5) prior art references have been combined to support the rejection of claims 62, 64-67. This alone, *i.e.*, the need to string together so many references, suggests that an obviousness rejection is not proper.

Claims 62, 64-67 are independent claims, and each has some similar limitations that generally relate to the storing or retrieving pixel data (or data elements) in parallel to or from a first and second memory.

For example, Claim 62 provides for retrieving pixel data for a first pixel and a second pixel in parallel from a first memory and a second memory, respectively, and retrieving pixel data for a third pixel and fourth pixel in parallel from the second memory and the first memory, respectively. The first, second, third and fourth pixels are located in the frame and are stored in the memory pages, for example, in a manner somewhat similar (but not identical) as that described above for claim 60. As discussed above in connection with claim 60, however, neither Reynolds, Takasugi nor Shreesha disclose this parallel retrieving as recited in claim 62 in recited fashion, and therefore claim 62 is also not rendered obvious by their combination. As will be explained below, the remaining two cited references should not be used in connection with this limitation either.

One of the references, Jones, was not discussed in the office action in any detail in connection with its applicability to claims 62, 64-67. Therefore, Applicants respectfully submit that there has been no *prima facie* showing by the Examiner in support of the obviousness rejection of these claims. A brief discussion of Jones appears on page 7 of the Office Action in connection with claim 5, but the Examiner made no reference of any relationship between claim 5 and claims 62, 64-67. Rather, claims 62, 63 - 67 were rejected under the same rationale as claims 7, 9, 10 - 13, 15 and 16 where Jones is part of a stated combination of Reynolds-Takasugi-Shreesha-Jones. However, there is no analysis of what limitations from claims 62, 63 - 67 appear in Jones, nor why Jones should be combined with Reynolds, Takasugi and Shreesha for the purposes of rejecting claims 62, 63 - 67.

Assuming however that the Examiner intended to incorporate his discussion of Jones for claim 5 into the grounds for rejecting claims 62, 64-67, Jones would not support such a rejection. Jones relates to a method for accessing different banks of a DRAM. A two dimensional image is organized in a two dimensional grid pattern of cells, where each cell contains a matrix of pixels. The words associated with each cell occupy one page or less of a bank. Each cell is assigned a particular one of the two banks so that all data words associated with that particular cell are read from and written to one particular page of that particular bank. The cited portions of Jones (cited in connection with claim 5) however do not disclose at least the parallel storing or retrieving (as the case may be) in the recited fashion of claims 62, 64-67, as the case may be.

Emmot discloses a method for allocating texture data sets, among first and second areas of memory in a computer graphics system. Each texture map in a series of texture maps is divided into a set of blocks of data. Blocks of data from first map areas of odd level texture maps and from the second map areas of even level texture maps are stored in the first memory area. Blocks of data from the second map areas of odd level texture maps and from the first map areas of even level texture maps are stored in the second memory area. The blocks of data representing each texture map in the series of texture maps are stored in consecutive blocks of memory. The cited portions of Emmot, however, do not disclose at least the parallel storing or retrieving (as the case may be) of claims 62, 64-67 in the recited fashion. Therefore, Emmot in combination with the other cited references do not render claims 62, 64-67 obvious.

Moreover, Applicant respectfully contends that it was not proper to combine Emmot with the other cited references. In order to combine references, the Examiner is required to show that there was a teaching, suggestion, or motivation to combine them. The reason given by the Examiner for combining Emmot is that it "reduces page miss penalty resulting in faster memory accesses." (Office Action, page 7). However as previously discussed, this is not a valid teaching, suggestion, or motivation. The recognition of a need does not render obvious the achievement that meets that need. Cardiac Pacemakers, Inc., v. St. Jude Medical, Inc., 381 F.3d 1371 (Fed. Cir. 2004).

In our case, the cited portions of Emmot generally deal with allocating texture data sets among first and second areas of memory in a computer graphics system to achieve faster memory accesses. However, the mere recognition of this need by Emmot does not render obvious Applicant's particular inventions in claims 62, 64-67 for achieving greater speed, *i.e.*, including the storing or retrieving (as the case may be) of consecutive data elements or pixels (as the case may be) in parallel in two different orders. Thus for this additional reason, independent claims 62, 64-67 are not obvious over Emmot in view of Reynolds, Takasugi, Shreesha, and Jones. Withdrawal of the rejections to claims 62, 64-67 is respectfully requested.

Claim 63 depends directly from claim 62, and includes all limitations of claim 62. Having established that claim 62 was not rendered obvious in view of the cited references,

dependent claim 63 similarly is not obvious. Withdrawal of the rejection to claim 63 also is requested.

Information Disclosure Statement

In reviewing Applicant's file history papers for this matter, Applicant notes that an Information Disclosure Statement ("IDS") was filed on or about April 8, 2002. However, it does not appear that the Examiner has returned an initialed IDS form for this submission. Moreover for some reason, this IDS does not even appear in the Patent Office's PAIR system.

Applicant thanks the Examiner for returning initialed IDS forms for Applicant's other IDS submission(s). However, Applicant respectfully requests that the Examiner kindly consider the references provided in the paper IDS filed April 8, 2002 and provide Applicant with an initialed copy indicating that the references were considered. For the Examiner's convenience, another copy of this paper IDS (along with a copy of the associated return receipt post card) is attached hereto.

CONCLUSION

For all the reasons advanced above, Applicant submits that the application is in a condition for allowance, and that action is earnestly solicited.

Respectfully submitted,

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